

ATTM6094

11 Mbit (256K x 44) Secondary Cache Module for R4000

Features

- 25 ns access time
- Support for 50 MHz R4000 MIPS architecture with zero wait-state
- High-speed CMOS SRAMs for cache data and tag functions
- Support for 16-, 32-, 64-, and 128-byte cache blocks
- Pin-compatible with IDT7MP6094 secondary cache module
- Single 5 V ($\pm 10\%$) power supply
- Gold-plated contacts on each side for minimum socket resistance
- Package styles available:
 - 80-lead SIMM module with surface-mount plastic components on epoxy (FR-4) substrate
 - TTL compatible I/Os
 - ZIP module

Description

The ATTM6094 is an 11 Mbit secondary cache module that supports the R4000 MIPS CPU. Four ATTM6094 modules are required to complete a full 4 Mbyte secondary cache for the R4000.

The module is constructed using eleven 256K x 4 high-speed CMOS SRAMs and two 10-bit buffer/drivers. The ICs are surface-mounted to an epoxy-glass laminate (FR-4) substrate. The 10-bit buffers incorporate on-chip 25 Ω series resistors that minimize overshoot and ringing during fast cycle times.

The ATTM6094 module is partitioned to provide both cache data and tag functions. Nine 256K x 4 bit SRAMs comprise the cache data while two 256K x 4 bit SRAMs are used for the tag and state. The ATTM6094 supports an R4000-based system at speeds to 50 MHz with zero wait-state operation. All inputs are TTL compatible and operate from a single 5 V supply.

The ATTM6094 module supports 16-, 32-, 64-, and 128-byte cache blocks via a jumper arrangement on addresses A0—A2 of the 128K x 8 tag and state SRAMs. The A0 address bypasses the 10-bit buffer pair. The standard module is wired for 16-byte cache blocks. The user may reconfigure the module by cutting PWB traces and installing wire jumpers as shown in Table 2.

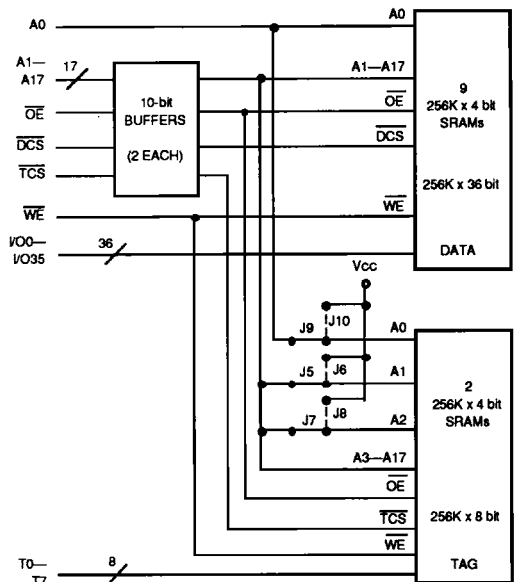


Figure 1. Block Diagram

Pin Information

Table 1. Pin Descriptions

Pin	Name/Function
I/O0—I/O35	Data Inputs/Outputs
T0—T7	Tag Inputs/Outputs
A0—A17	Address Inputs
$\overline{\text{DCS}}$	Data Chip Select
$\overline{\text{TCS}}$	Tag Chip Select
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	No Connect

Table 2. Jumper Combinations (J5—J9)*
(See Figure 1.)

Jumper	Jumper Type	Second-Level Cache Block Size (Bytes)			
		16*	32	64	128
J5	Trace	In	In	Cut	Cut
J6	Wire	Out	Out	In	In
J7	Trace	In	In	In	Cut
J8	Wire	Out	Out	Out	In
J9	Trace	In	Cut	Cut	Cut
J10	Wire	Out	In	In	In

* The standard module configuration provides 16-byte cache blocks and nonbuffered A0 address. The user may reconfigure the module by cutting PWB traces and installing wire jumpers as shown.

Note: Jumpers J1—J4 (not shown) are factory set. There are no address buffer options.

GND	1	2	Vcc
I/O0	3	4	I/O1
I/O2	5	6	I/O3
I/O4	7	8	I/O5
I/O6	9	10	GND
I/O7	11	12	I/O8
I/O9	13	14	I/O10
I/O11	15	16	I/O12
I/O13	17	18	I/O14
GND	19	20	I/O15
I/O16	21	22	I/O17
I/O18	23	24	I/O19
I/O20	25	26	I/O21
I/O22	27	28	GND
Vcc	29	30	I/O23
I/O24	31	32	I/O25
I/O26	33	34	I/O27
I/O28	35	36	I/O29
GND	37	38	I/O30
I/O31	39	40	I/O32
I/O33	41	42	I/O34
I/O35	43	44	GND
$\overline{\text{WE}}$	45	46	A0
A1	47	48	A2
A3	49	50	A4
A5	51	52	A6
GND	53	54	Vcc
$\overline{\text{DCS}}$	55	56	$\overline{\text{OE}}$
A7	57	58	A8
A9	59	60	A10
A11	61	62	GND
A12	63	64	A13
A14	65	66	A15
A16	67	68	A17
$\overline{\text{TCS}}$	69	70	T0
GND	71	72	T1
T2	73	74	T3
T4	75	76	T5
T8	77	78	T7
Vcc	79	80	GND

Note: Pins alternate side-to-side on the ZIP module (as shown). All 80 pins on the SIMM module appear on both sides.

Figure 2. Pin Diagram (Top View)

Application

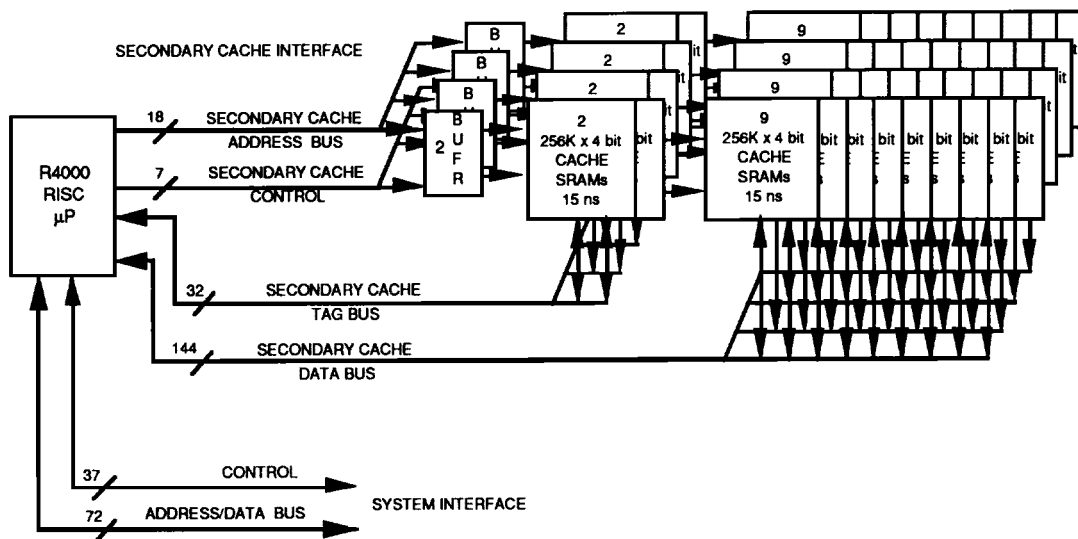


Figure 3. Typical R4000 Secondary Cache Application (4 Mbyte Cache Consisting of Four ATTM6094 Modules)

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Terminal Voltage with Respect to GND	V _{TERM}	-0.5	7.0	V
Operating Temperature	T _A	0	70	°C
Storage Temperature	T _{stg}	-55	125	°C
dc Output Current (Short Circuit)	I _{OUT}	—	25	mA

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Commercial	0 °C to 70 °C	5 V ± 10%

Electrical Characteristics

Table 3. General Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage:						
High	V _{IH}	—	2.2	—	V _{CC} + 0.3	V
Low	V _{IL}	—	-0.5	—	0.8	V
Output Voltage:						
High	V _{OH}	V _{CC} = Min, I _{OH} = -4 mA	2.4	—	—	V
Low	V _{OL}	V _{CC} = Min, I _{OL} = 8 mA	—	—	0.4	V
Supply Voltage	V _{CC}	—	4.5	5	5.5	V
Ground	GND	—	0	0	0	V
Input Leakage Current:						
Except A0, <u>WE</u>	I _{LI1}	V _{CC} = Max, V _{IN} = GND to V _{CC}	—	—	10	μA
A0, <u>WE</u>	I _{LI2}	V _{CC} = Max, V _{IN} = GND to V _{CC}	—	—	110	μA
Output Leakage Current	I _{LO}	V _{CC} = Max, <u>CS</u> = V _{IH} , V _{OUT} = GND to V _{CC}	—	—	10	μA
Operating Current ^{1,2} (typical R4000 application)	I _{CC}	—	—	—	490	mA
Standby Current ³	I _{SB}	—	—	—	300	mA
Active Current (100% duty cycle)	I _{MAX}	Inputs changing 0 V—3 V; Outputs open; DCS = TCS = WE = low; Write cycle = 50 ns	—	—	1250	mA
Capacitance: ¹						
Input/Output (data)	C _{IO} (D)	V _{IN} = 0 V	—	—	10	pF
Input (A1—A15, OE, TCS, DCS)	C _{IN} (A)	V _{IN} = 0 V	—	—	10	pF
Input (A0, WE)	C _{IN} (B)	V _{IN} = 0 V	—	—	100	pF

1. This parameter is guaranteed by design, but not tested.

2. The conditions for determining operating current (I_{CC}) for a typical R4000 system are as follows:

- 50 MHz master clock.
- 100 MHz (internal) Pclock.
- Assume 5 Pclock cycles required for a secondary cache read or write; therefore, min. read/write cycle = 50 ns and min. access time (module) = 25 ns.
- Assume hit rate of primary cache is 85%; therefore, secondary cache has 15% duty cycle for read/write instructions from the R4000 processor.
- Allow an additional 5% module duty cycle for secondary cache fill and copyback operations; therefore, total secondary cache duty cycle is 20%.

Under the conditions outlined above, the maximum operating current for the module is 490 mA:

$$I_{CC} = (\%active)(I_{MAX}) + (\%standby)(I_{SB})$$

$$I_{CC} = (0.20 \times 1250 \text{ mA}) + (0.80 \times 300 \text{ mA})$$

$$I_{CC} = 490 \text{ mA}$$

3. Tested with outputs open and all address and data inputs stable. The module is continuously disabled (TCS = DCS = V_{CC}). Input levels are within 0.2 V of V_{CC} or ground.

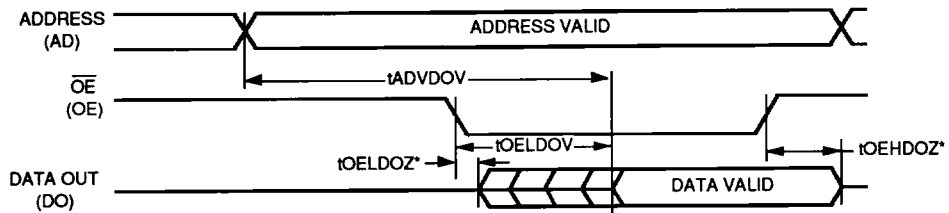
Timing Characteristics

Table 4. Read Cycle

$V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$

Symbol	Parameter	Min	Max	Unit
tADVDOV	Address Access Time	—	25	ns
tOELDOV	Output Enable to Output Valid	—	25	ns
tOEHDZ*	Output Enable High to Output in High Z	—	20	ns
tOELDOZ*	Output Enable to Output in Low Z	0	—	ns

*This parameter is guaranteed by design, but not tested.



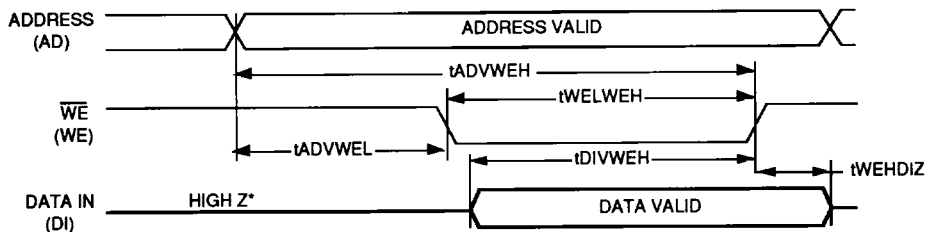
*This parameter is guaranteed by design, but not tested.

Figure 4. Read Cycle

Table 5. Write Cycle

$V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$

Symbol	Parameter	Min	Max	Unit
tADVWEH	Address Valid to End of Write	25	—	ns
tWELWEH	Write Pulse Width	15	—	ns
tDIVWEH	Data Valid to End of Write	10	—	ns
tWEHDIZ	Data Hold Time	0	—	ns
tADVWEL	Address Valid to Write Enable Low	7	—	ns



* Common I/O lines must be in 3-state prior to a write cycle.

Figure 5. Write Cycle

Timing Characteristics (continued)

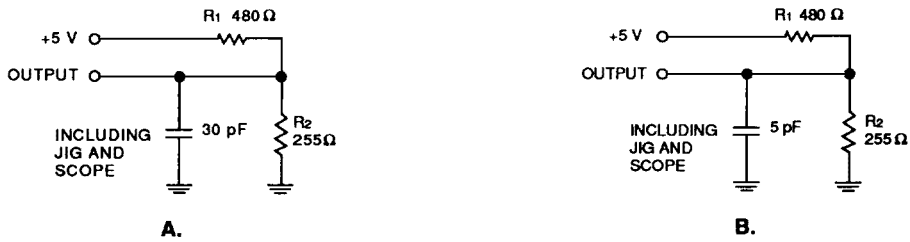


Figure 6. Test Loads

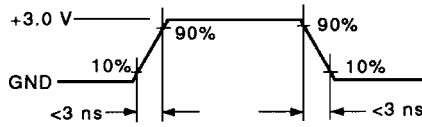
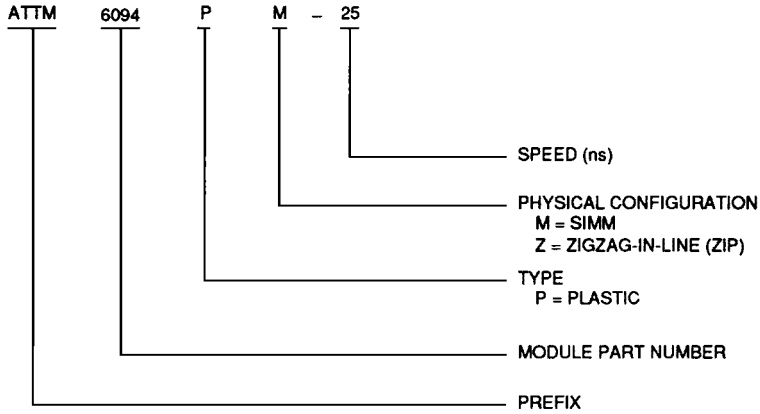


Figure 7. Transition Times

Ordering Information



Operating Range 0 °C to 70 °C on all devices.

Device #	Package Style	Performance Speed
		25 ns
ATTM6094	80-Lead SIMM Module	ATTM6094PM-25
	80-Lead ZIP Module	ATTM6094PZ-25