PWR-SMP402

1-Watt Buck Regulator IC

20-72 VDC Input
Non-isolated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power > 1 W from 48 VDC input
- Adjustable output voltage
- Integrated solution minimizes overall size

High-voltage, Low-capacitance MOSFET Output
- Designed for ISDN T1 telecommunications applications
- Low capacitance allows for high frequency operation

High-voltage Buck Regulator
- Internal pre-regulator self-powers the IC on start-up
- Designed for low power consumption
- Minimum external parts required

Built-In Self-protection Circuits
- Undervoltage lockout
- Thermal shutdown
- Input polarity/level sense

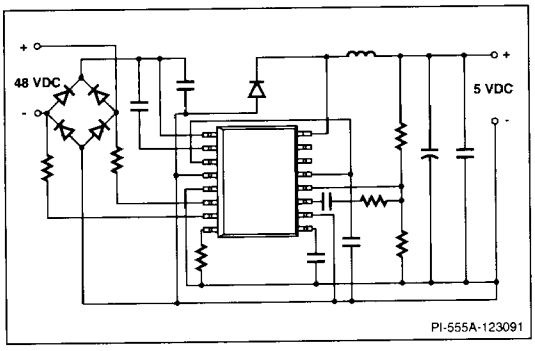

Figure 1. Typical Application.

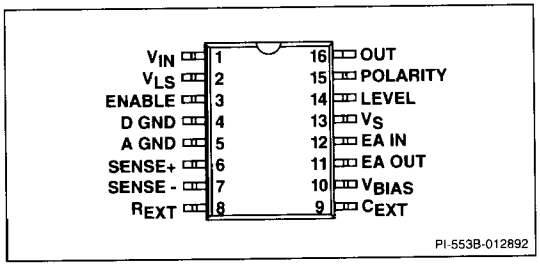

Figure 2. Pin Configuration.

Description

The PWR-SMP402, intended for non-isolated ISDN telecommunications power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost power supply which meets stringent ISDN specifications. High frequency operation reduces total power supply size.

The P-channel power MOSFET switch features include high voltage, low $R_{DS(ON)}$, and low capacitance. Lower capacitance results in a reduction in gate drive power, and also facilitates higher frequency operation.

The controller section of the PWR-SMP402 contains all the blocks required to drive and control the power stage: start-up pre-regulator circuit, oscillator, bandgap reference, error amplifier, gate driver and level shift. Protection features include undervoltage lockout, thermal shutdown, and input polarity and level sensing.

The PWR-SMP402 is available in a 16-pin plastic SOIC package.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP402TNC	16-pin SOIC	0 to 70°C

Pin Functional Description

Pin 1:
V_{IN} is the high-voltage input to the switching regulator. This is the Source connection of the P-Channel power MOSFET pass transistor.

Pin 2:
V_{LS} is an internal supply for the level shift circuit that drives the P-Channel MOSFET. A capacitor should be placed between V_{LS} and V_{IN} for bypassing. V_{LS} is normally 10 V below V_{IN}.

Pin 3:
The power supply can be shut down by pulling **ENABLE** low.

Pin 4:
D GND is the common return point for the logic portions of the circuit.

Pin 5:
A GND is the common return point. R_{EXT} and C_{EXT} are directly connected to this point.

Pin 6:
The **SENSE+** input monitors the polarity and level of the input voltage for ISDN emergency standby sensing.

Pin 7:
The **SENSE-** input monitors the polarity and level of the input voltage for ISDN emergency standby sensing.

Pin 8:
A 20.5 kΩ resistor connected between R_{EXT} and A GND sets the internal bias currents including oscillator charge and discharge currents.

Pin 9:
The oscillator frequency can be programmed by selecting the value of the capacitor connected between C_{EXT} and A GND.

Pin 10:
V_{BIAS} can be connected to the output 5 V rail of the converter to reduce power dissipation. The internal 5 V regulator is cut off when the output is in regulation.

Pin 11:
EA OUT is the error amplifier output pin for connection to the external compensation network.

Pin 12:
EA IN is the error amplifier negative input for connection to the feedback and compensation networks.

Pin 13:
V_S is the internal supply voltage. This pin is brought out for external bypassing.

Pin 14:
The **LEVEL** output indicates when the input voltage is in its normal operating range.

Pin 15:
The **POLARITY** output is used to notify a microprocessor of an emergency standby condition for ISDN applications.

Pin 16:
OUT is the Drain connection of the P-Channel pass transistor.

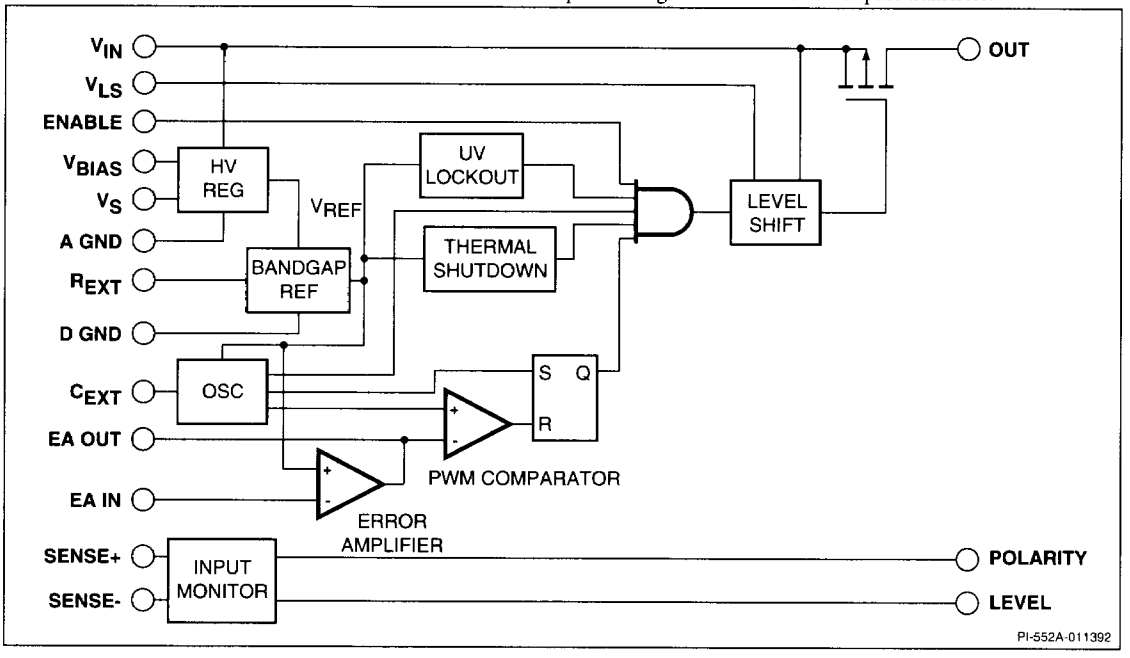

Figure 3. Functional Block Diagram.

Functional Description

High Voltage Regulator

The high-voltage regulator provides the bias current required by the controller and driver circuitry. The pre-regulator consists of a high voltage MOSFET, a gate bias current source, and an error amplifier. The error amplifier regulates V_S to approximately 5 volts by controlling the gate of the MOSFET.

In 5 V output applications, the control circuitry may also be operated by connecting the V_{BIAS} pin to the output 5 V rail of the converter to reduce power dissipation. The internal 5 V regulator is cut off automatically when the converter output is in regulation. Only the supply current for the level shift stage (≈50 µA) and the AC switching currents for the P-Channel output device are drawn from the V_{IN} supply under this condition. If unused, V_{BIAS} must be hardwired to A GND to disable the automatic switchover during powerup.

V_{LS} is the level-shift supply for driving the gate of the internal P-channel MOSFET. The voltage at V_{LS} is approximately 10 V below V_{IN}. V_S is the supply voltage for the controller and driver circuitry. External bypass capacitors connected to V_{LS} and V_S are required for filtering and reducing noise.

UV Lockout

During powerup, the Undervoltage Lockout circuit keeps the P-channel output transistor in the off state until the internal V_S supply is in regulation and the voltage sensed by the input monitor circuit is within the normal operation range (>20 V).

Band Gap Reference

V_{REF} is the 1.25 V reference voltage generated by the temperature-compensated bandgap reference and buffer. This voltage is used for setting thresholds for the error amplifier and over temperature circuit.

Oscillator

The oscillator frequency can be adjusted by changing the external C_{EXT} capacitor. This capacitor is charged and discharged by switched constant current sources.

The voltage switch points are determined by hysteresis built into a comparator. The period of the waveform is determined by values of the current sources which set the rising and falling slopes of the sawtooth waveform. Maximum duty cycle is equal to the ratio of the charge time to the period. Clock and blanking signals are synthesized from the comparator output for use by the modulator.

Error Amplifier

The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch.

Pulse Width Modulator

The pulse width modulator implements a voltage-mode control loop, and generates the digital driver signal which controls the power switch. The duty cycle of the driver signal will change as a function of input voltage and load. Increasing the duty cycle causes the power supply output voltage to go up. Conversely, decreasing the duty cycle causes the output voltage to go down. The pulse width modulator compares the control voltage (error amplifier output) with the sawtooth voltage generated by the oscillator to produce the required duty cycle.

Thermal Shutdown

Temperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 140°C). The device will automatically reset and turn back on again when the junction has cooled past the hysteresis temperature level.

Input Polarity and Level Sense

The input monitor circuitry checks the input voltage polarity. The inputs to the circuit are SENSE+ and SENSE-, low impedance input nodes biased at approximately 1.5 V and externally connected by dropping resistors to the high-voltage input.

POLARITY is a logic-level output that indicates the input voltage polarity. When the input voltage is normal, POLARITY is high, and when the input voltage is reversed, POLARITY is low. This output is only valid after the output voltage is in regulation.

The LEVEL output indicates the input voltage level as defined by the two sensing resistors R_{S+} and R_{S-}. It is valid only after the output voltage is in regulation. Since the internal undervoltage lockout is set at 20 V, it is recommended that the LEVEL input be set at no less than 24 V for proper operation.

Enable

The power supply can be shut down by pulling the ENABLE pin low. It is internally pulled up to V_S with a 100 µA (nominal) current source. However, it is recommended that this pin be tied to V_S if it is unused.

P-Channel Output Transistor

The output MOSFET is a 90 V pass transistor capable of supplying >200 mA. To minimize switching noise and EMI, it is important to keep the path from OUT through the output diode, the input storage capacitor, and into V_{IN} as short as possible.

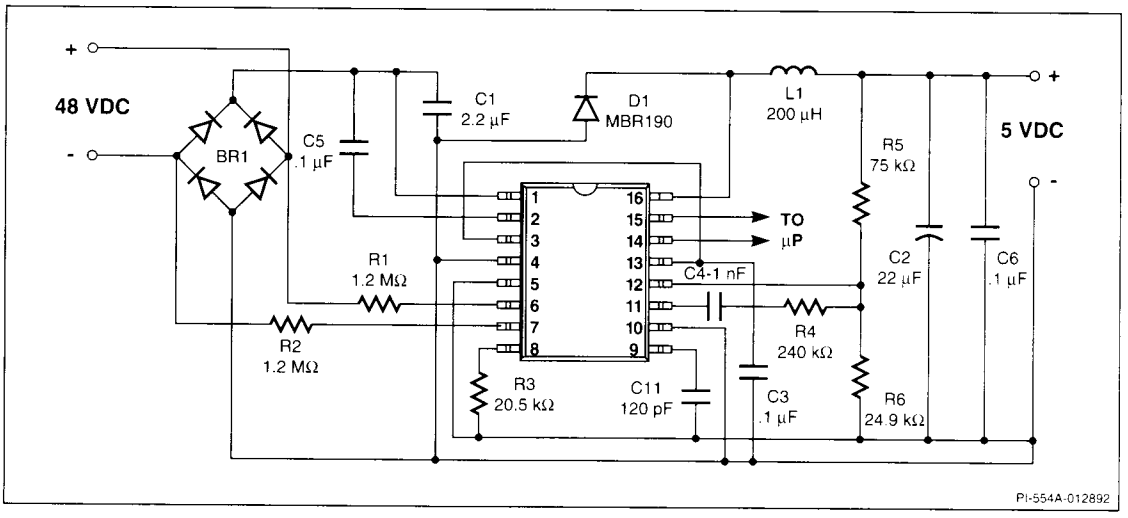

Figure 4. Non-isolated ISDN Regulator Circuit.

General Circuit Operation

The buck regulator power supply circuit shown in Figure 4 will produce a 5 volt, 1 watt power supply that will operate over a 20 to 72 VDC input voltage range. The output voltage is selected by the resistor divider ratio formed by R5 and R6. The maximum output voltage is limited to 50% of the minimum DC input voltage by the maximum duty cycle and the voltage drop across the switch when it is on.

$$V_O = 1.25 \times \frac{R_5 + R_6}{R_6}$$

The P-channel switch inside the integrated circuit, D1, L1, and C2 form the buck regulator power processing path. The P-channel switch and D1 chop the DC input voltage with a duty cycle that changes the average voltage to be equal to the output voltage and L1 and C2 form the low pass filter that extracts the average value and rejects the AC components of the switching waveform.

R4, R5, and C4 are the frequency compensation components for the output error amplifier and affect the stability of the control loop. The values of these components are related to the low pass filter elements L1 and C2.

C11 sets the oscillator frequency. The frequency is inversely proportional to the capacitance value and is nominally 200 kHz when using a 120 pF capacitor. R3 sets the internal current sources within the integrated circuit. The value of R3 is fixed.

C3 and C5 are bypass capacitors that supply transient currents within the integrated circuit. C5 bypasses the P-channel gate drive circuit . C1 is the input filter capacitor. C1 averages the pulsing current that flows through the P-channel switch to reduce the EMI feedback to the DC voltage source. C1 also stores energy to sustain the output voltage for short interruptions in the DC input voltage.

R1 and R2 are used to sense the polarity of the input voltage for ISDN applications. A reversed battery voltage indicates emergency standby battery operation. The POLARITY signal allows the control logic in the integrated circuit to notify the load when this occurs. The input voltage at which LEVEL notifies the load that an undervoltage condition occurs can be selected by the values of R1 and R2.

The circuit also has an enable input that allows the output voltage to be turned off with a logic signal. This signal is normally generated by the logic circuitry in the load circuit, and turns off non-essential loads and/or functions when an emergency battery condition exists.

ABSOLUTE MAXIMUM RATINGS[1]

V_{IN} Voltage	90 V
Drain-Source Voltage (V_{IN} to OUT)	90 V
V_{BIAS} Voltage	5.5 V
SENSE Current	±200 µA
OUT Current	250 mA
Logic Input Voltage	-0.3 V to V_S + 0.3 V
Storage Temperature	–65 to 165°C
Ambient Temperature	0 to 70°C
Junction Temperature	150°C
Lead Temperature[2]	260°C
Power Dissipation	1.0 W
Thermal Impedance (θ_{JA})	100°C/W

1. Unless noted, all voltages referenced to A GND, T_A=25°C.
2. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 48 V, V_{BIAS} = 5 V, GNDs = 0V, R_{EXT} = 20.5 kΩ, C_{EXT} = 120 pF, R_{S+}, R_{S-} = 1.2 MΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Output Frequency	f_{OSC}	C_{EXT} = 30 to 300 pF	50		500	kHz
Initial Accuracy	Δf_{OSC}		170	200	230	kHz
PULSE WIDTH MODULATOR						
Duty Cycle	DC		0-50	0-60		%
ERROR AMPLIFIER						
Threshold Voltage	V_{REF}		1.25		1.35	V
Gain-Bandwidth Product				0.5		MHz
DC Gain	A_{VOL}		60	80		dB
Output Impedance	Z_{OUT}			1		kΩ
CIRCUIT PROTECTION						
Thermal Shutdown Temperature			120	140		°C
Thermal Shutdown Hysteresis				15		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 48 V, V_{BIAS} = 5 V, GNDs = 0V, R_{EXT} = 20.5 kΩ, C_{EXT} = 120 pF, R_{S+}, R_{S-} = 1.2 MΩ, T_A = 0 to 70°C		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
LOGIC							
Input Current High	I_{IH}				10	50	µA
Input Current Low	I_{IL}				100	500	µA
Input Voltage High	V_{IH}					3.0	V
Input Voltage Low	V_{IL}			1.0			V
Output Voltage High	V_{OH}	I_{OH} = -0.5 mA		3.5			V
Output Voltage Low	V_{OL}	I_{OL} = 0.5 mA				0.4	V
SENSE INPUTS							
POLARITY Threshold Voltage		See Figure 5			0		V
LEVEL Threshold Current		See Figure 5			23		µA
LEVEL Current Hysteresis		See Figure 5			3		µA
LEVEL Bias Voltage		See Figure 5			1.7		V
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_{OUT} = -100 mA	T_J = 25°C			12	Ω
			T_J = 115°C			20	
ON-State Current	$I_{D(ON)}$	See Note 1		200			mA
OFF-State Current	I_{DSS}	OUT = 72 V, T_A = 115°C			10	50	µA
Breakdown Voltage	BV_{DSS}	I_{OUT} = -100 µA, T_A = 25°C		90			V

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 48 V, V_{BIAS} = 5 V, GNDs = 0V R_{EXT} = 20.5 kΩ, C_{EXT} = 120 pF R_{S+}, R_{S-} = 1.2 MΩ, T_A = 0 to 70°C	Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
SUPPLY						
HV Regulator Voltage	V_{IN}		20		72	V
Off-line Supply Current	I_{IN}	V_{BIAS} = A GND			2.5	mA
		V_{BIAS} = 5 V			1.5	
V_{BIAS} Supply Voltage	V_{BIAS}		4.75		5.25	V
V_{BIAS} Supply Current	I_{BIAS}			1		mA

NOTES:

1. At low output currents (< 20 mA), the part may operate in blocking oscillation mode, resulting in large output ripple.

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INPUT VOLTAGE CONDITION	POLARITY	LEVEL
Negative voltage, level too low	0	0
Negative voltage, correct level	0	1
Positive voltage, level too low	1	0
Positive voltage, correct level	1	1

Figure 5. LEVEL/POLARITY Input-Output Truth Table.