

The RF Line

921 MHz - 960 MHz SiFET

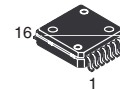
RF Integrated Power Amplifier

The MHVIC910HR2 integrated circuit is designed for GSM base stations, uses Motorola's newest High Voltage (26 Volts) LDMOS IC technology, and contains a three-stage amplifier. Target applications include macrocell (driver function) and microcell base stations (final stage). The device is packaged in a PFP-16 Power Flat Pack package which gives excellent thermal performances through a solderable backside contact.

- Typical GSM Performance @ Full Frequency Band (921 - 960 MHz), 26 Volts
Output Power - 40 dBm (CW) @ P1dB
Power Gain - 39 dB @ P1dB
Efficiency - 48% @ P1dB
- Integrated ESD Protection
- Usable Frequency Range - 921 to 960 MHz
- Available in Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.

MHVIC910HR2

960 MHz, 10 W, 26 V
GSM CELLULAR
RF LDMOS INTEGRATED CIRCUIT



CASE 978-03
(PFP-16)

MAXIMUM RATINGS

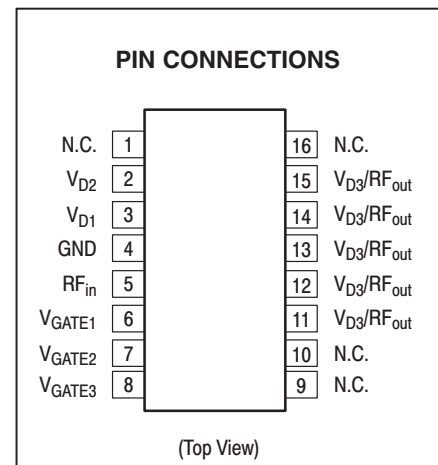
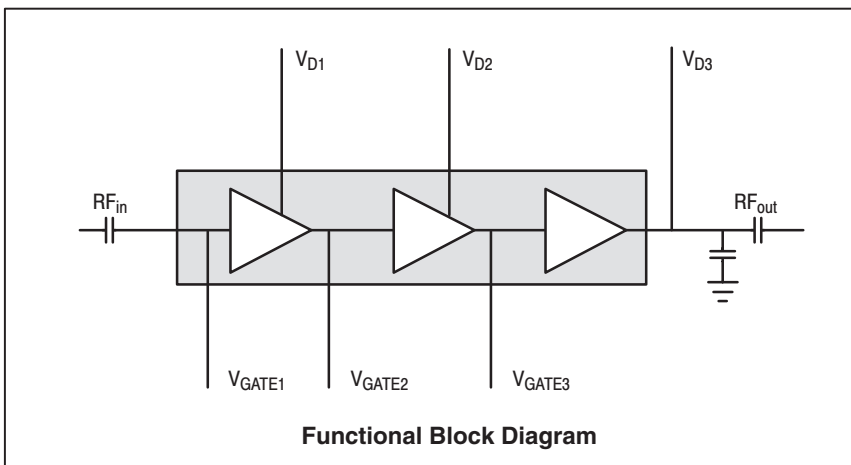
Rating	Symbol	Value	Unit
Drain Supply Voltage	V_{DD}	28	Vdc
Gate Supply Voltage	V_{GS}	6	Vdc
RF Input Power	P_{in}	5	dBm
Case Operating Temperature	T_C	- 30 to + 85	°C
Storage Temperature Range	T_{stg}	- 65 to + 150	°C
Operating Channel Temperature	T_{ch}	150	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	0 (Minimum)
Machine Model	M2 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.9	°C/W



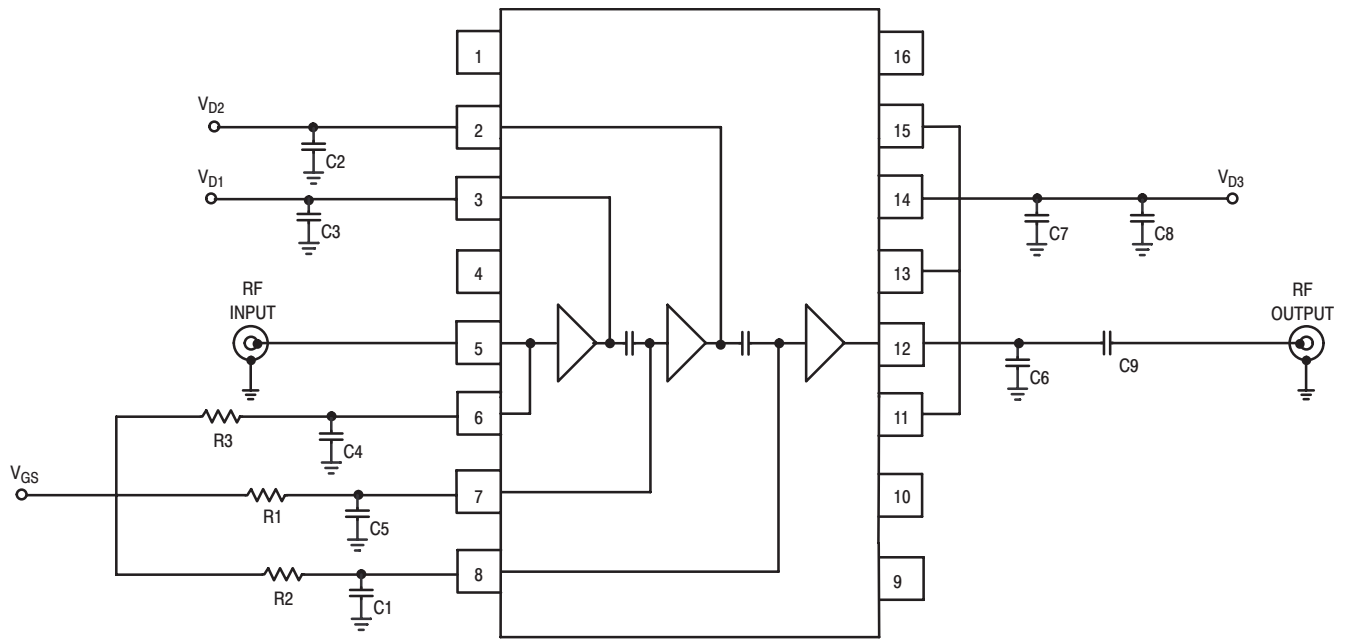
NOTE: MHVIC910HR2 Moisture Sensitivity Level (MSL) = 3.

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
Drain Supply Voltage	V_{DD}	26	Vdc
3rd Stage Quiescent Current	I_{DQ3}	150	mA
2nd Stage Quiescent Current	I_{DQ2}	50	mA
1st Stage Quiescent Current	I_{DQ1}	25	mA

ELECTRICAL CHARACTERISTICS ($V_{DD} = 26$ V, V_{GS} set for $I_{DQ3} = 150$ mA, $T_A = 25^\circ\text{C}$ matched to a $50\ \Omega$ system, frequency range 921 – 960 MHz, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	f_{RF}	921	—	960	MHz
Output Power @ 1 dB Compression Point	P @ 1dB	39	40	—	dBm
Power Gain @ P1dB	G @ 1dB	38	39	—	dB
Power Added Efficiency @ 1 dB Compression Point	PAE @ 1dB	43	48	—	%
Input Return Loss @ P1dB	IRL @ 1dB	—	-15	-10	dB
Gain Flatness @ 40 dBm Variation ($T_C = -30$ to $+85^\circ\text{C}$ @ 40 dBm)	G_F G_V	— —	.5 5	— —	dB dB
Load Stability ($V_{DS} = 24$ V to 28 V, $P_{out} = \text{P1dB Down to } 0$ dBm, All Phase Angles)	VSWR	10:1	—	—	—
Ruggedness ($V_{DS} = 26$ V, $P_{out} = 42$ dBm, Load VSWR = 10:1, All Phase Angles)	Ψ	No Damage After Test			



- | | | | |
|------------------------|--|------------|---------------------------------------|
| C1, C2, C3, C4, C5, C8 | 1 μ F Surface Mount Chip Capacitors | J1, J2 | Header (Break-away), HDR2X10STIMCSAFU |
| C6 | 4.7 pF AVX Chip Capacitor, ACCU-P (08051J4R7BBT) | J3, J4 | SMA Connector 2052-1618-02 (Threaded) |
| C7 | 47 pF AVX Chip Capacitor, ACCU-P (08055K470JBTR) | R1, R2, R3 | 100 Ω Chip Resistors (0402) |
| C9 | 33 pF AVX Chip Capacitor, ACCU-P (08053J330JBT) | PCB | Rogers 04350, 20 mils |

Figure 1. 921-960 MHz Demo Board Schematic

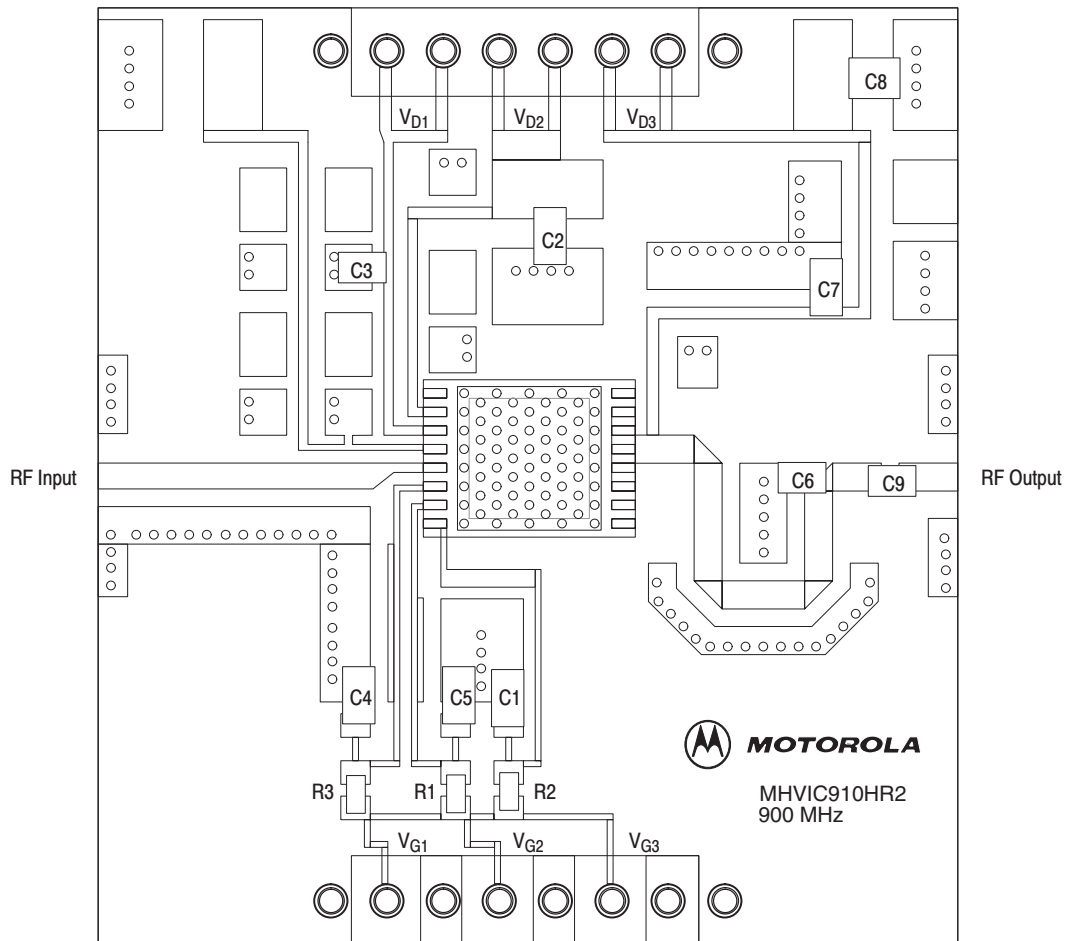


Figure 2. 921-960 MHz Demo Board Component Layout

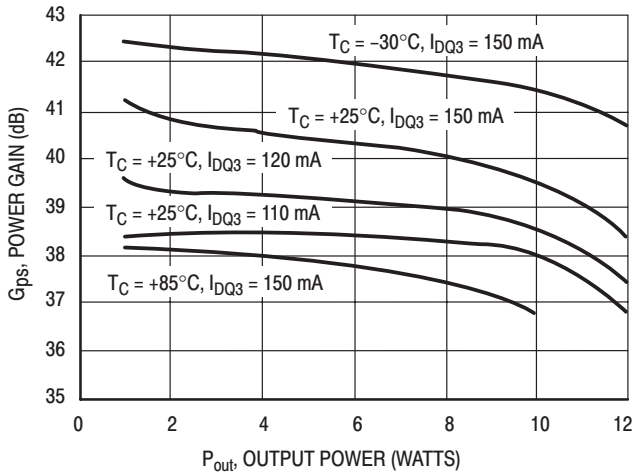


Figure 3. Power Gain versus Output Power

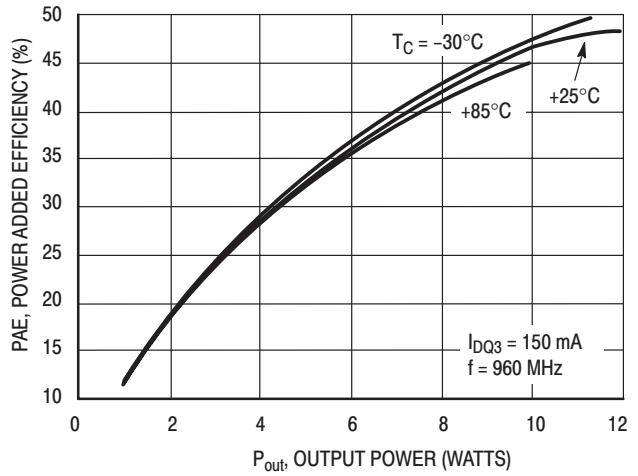


Figure 4. Power Added Efficiency versus Output Power

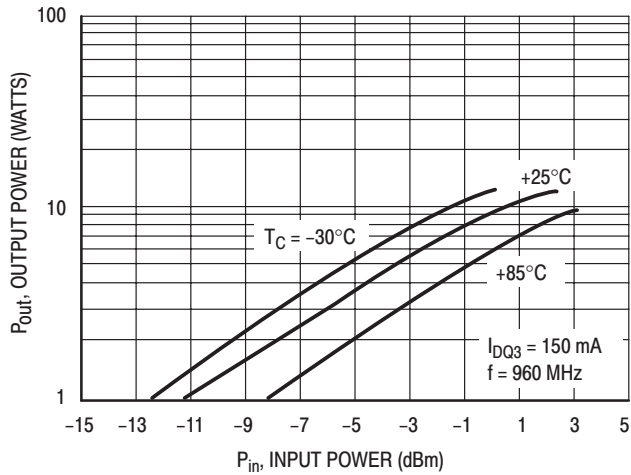


Figure 5. Output Power versus Input Power

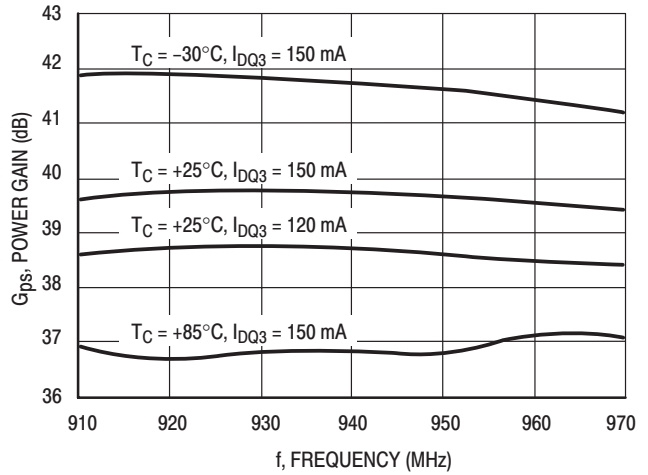


Figure 6. Power Gain versus Frequency
 $P_{out} = 10\text{ W}$

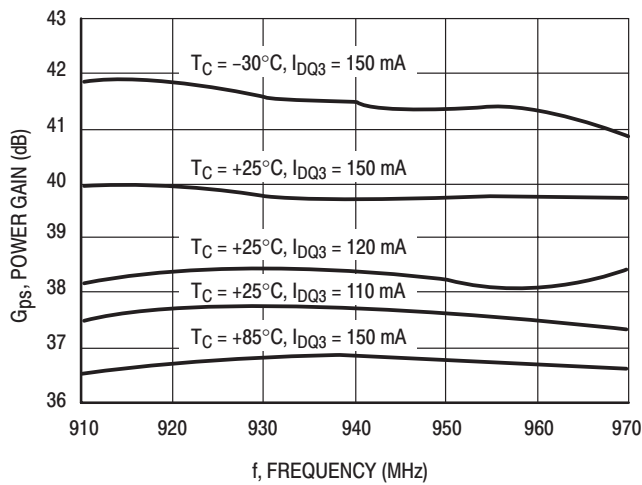


Figure 7. Power Gain versus Frequency
 $P_{out} = P1dB$

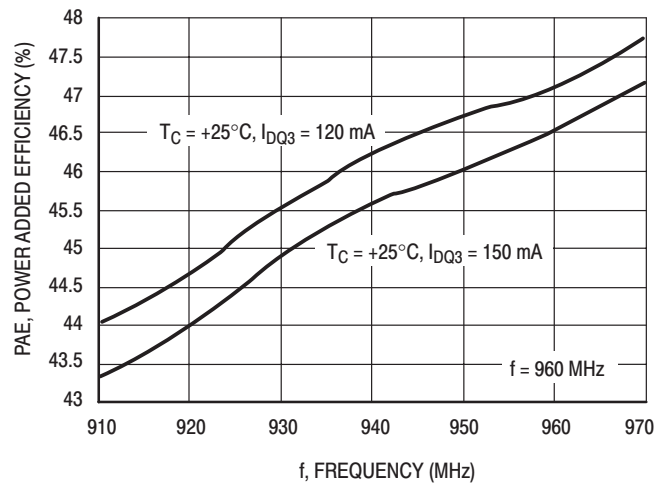


Figure 8. Power Added Efficiency versus Frequency
 $P_{out} = 10\text{ W}$

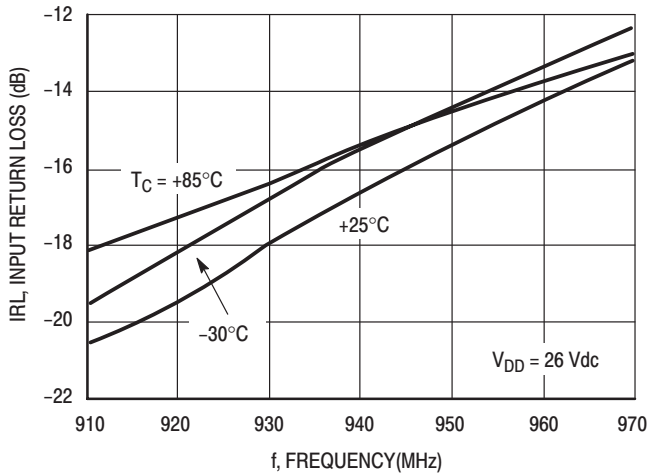


Figure 9. Input Return Loss versus Frequency
 $P_{out} = 10\text{ W}$

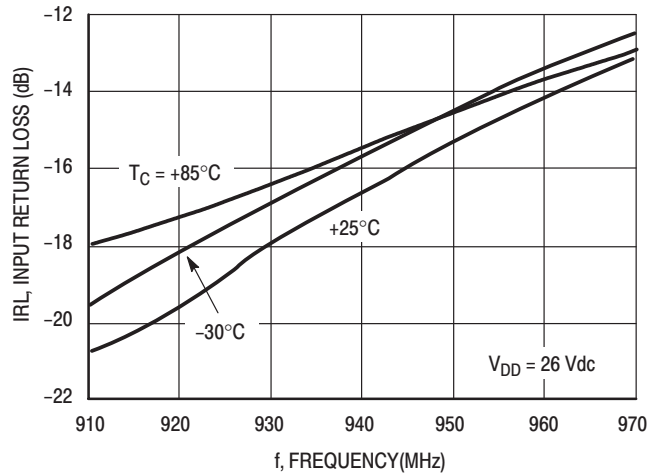


Figure 10. Input Return Loss versus Frequency
 $P_{out} = P1dB$

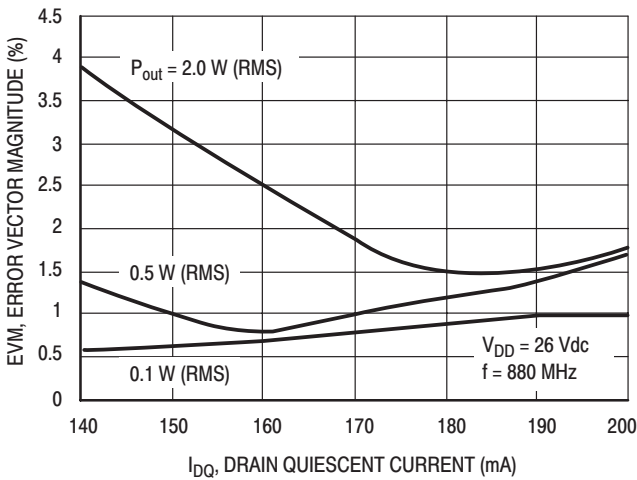


Figure 11. Error Vector Magnitude versus I_{DQ} Total

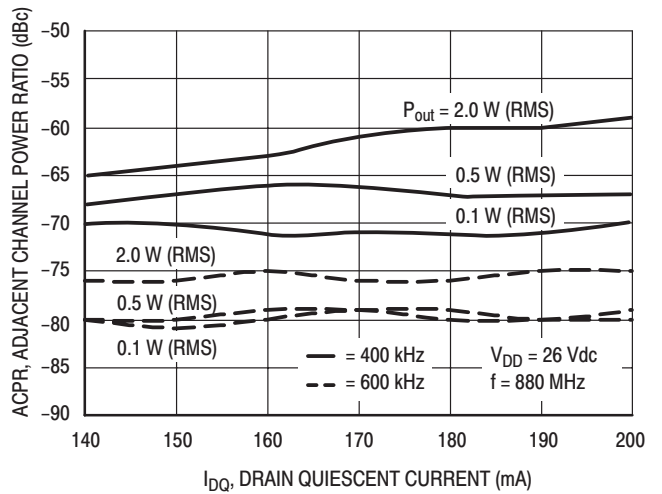


Figure 12. Adjacent Channel Power Ratio versus I_{DQ} Total

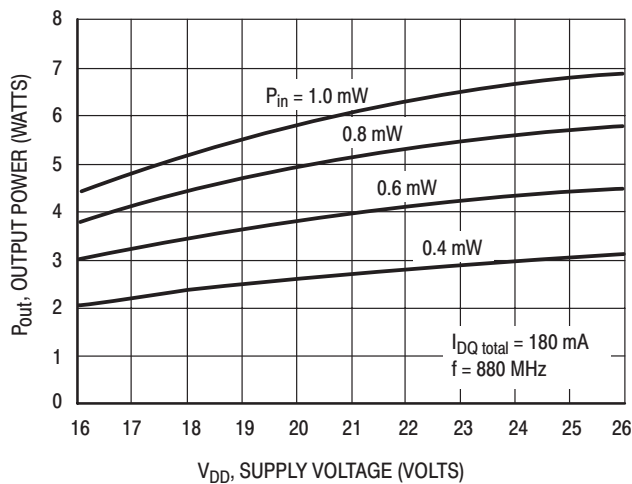


Figure 13. Output Power versus Supply Voltage

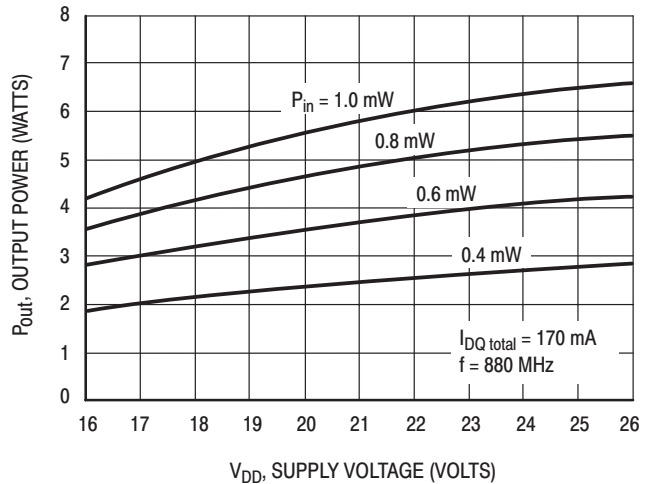


Figure 14. Output Power versus Supply Voltage

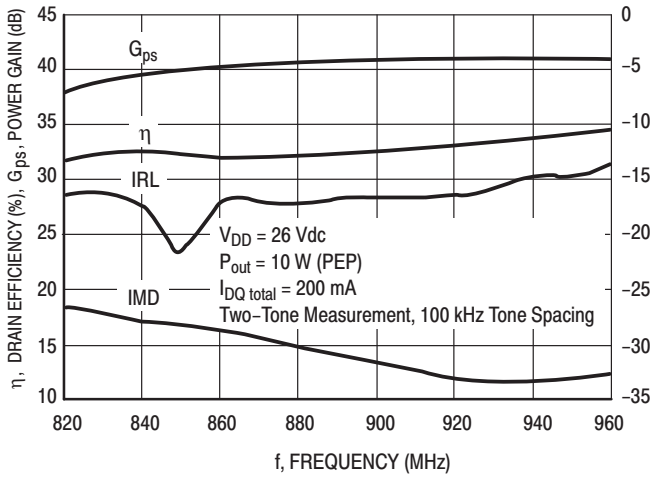


Figure 15. Two-Tone Broadband Performance

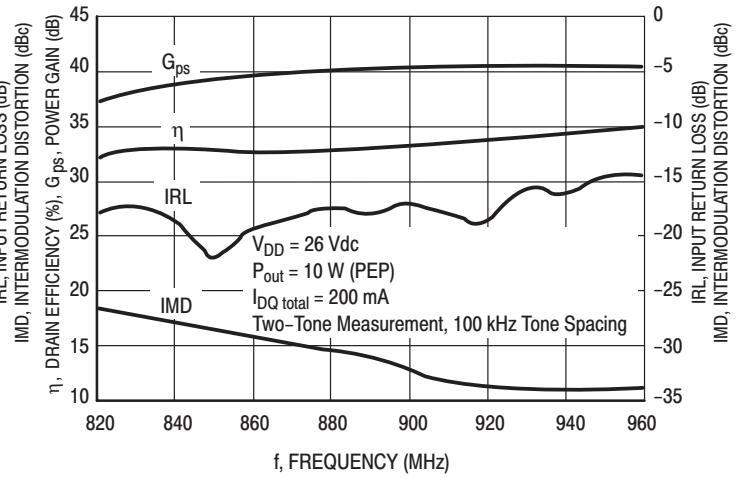


Figure 16. Two-Tone Broadband Performance

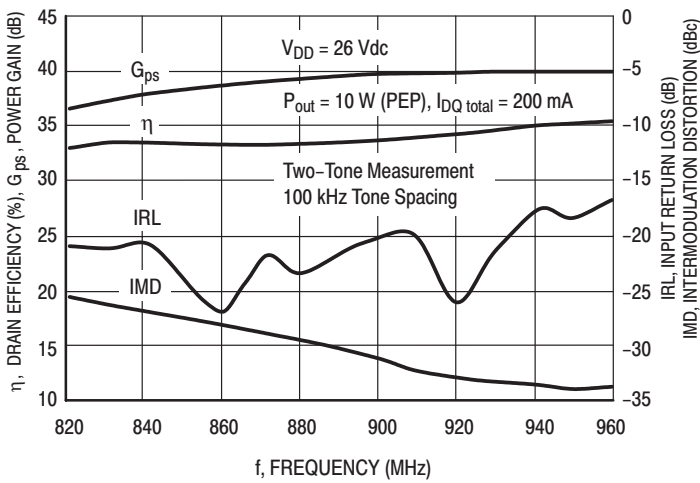


Figure 17. Two-Tone Broadband Performance

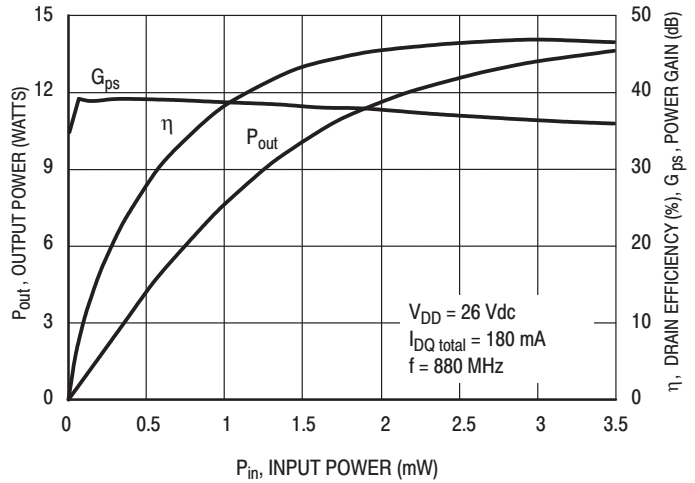


Figure 18. CW Performance @ 880 MHz

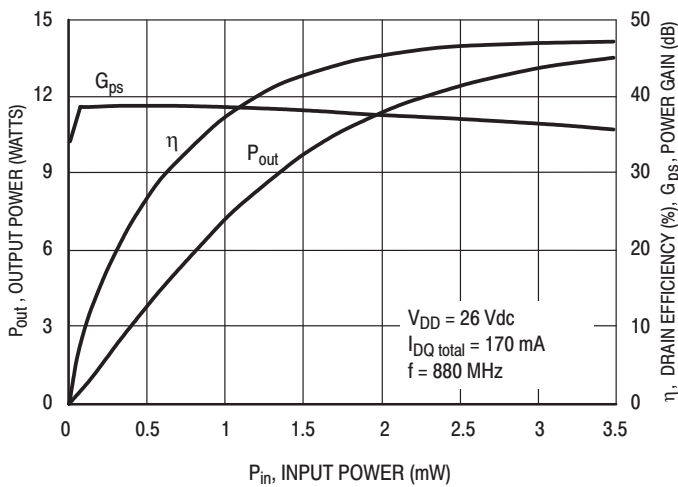


Figure 19. CW Performance @ 880 MHz

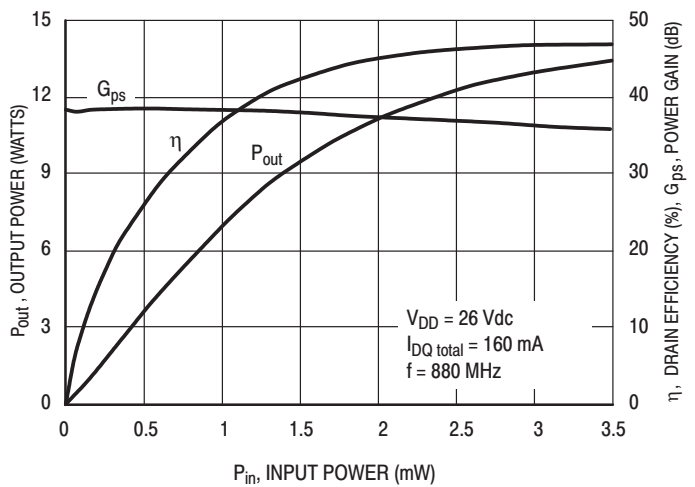


Figure 20. CW Performance @ 880 MHz

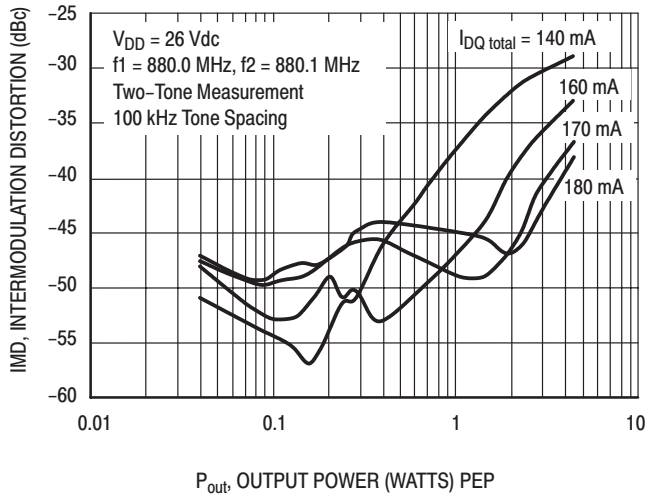
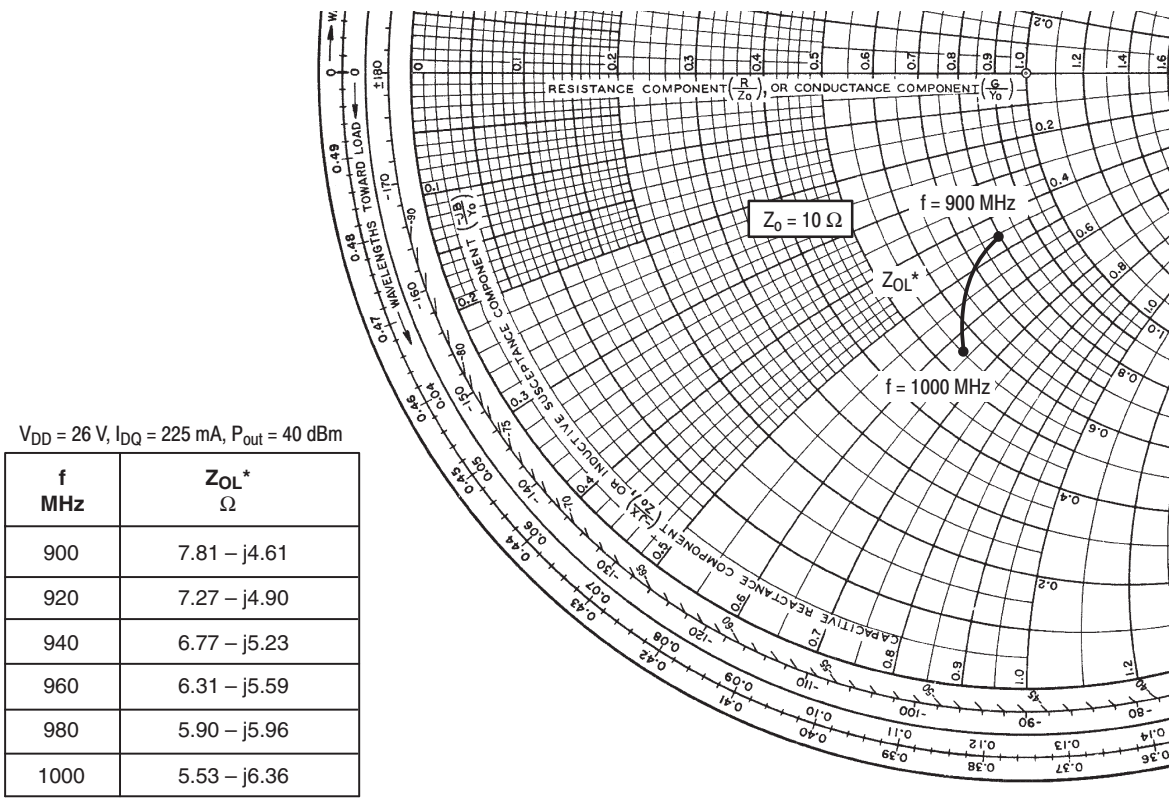


Figure 21. Intermodulation Distortion versus Output Power

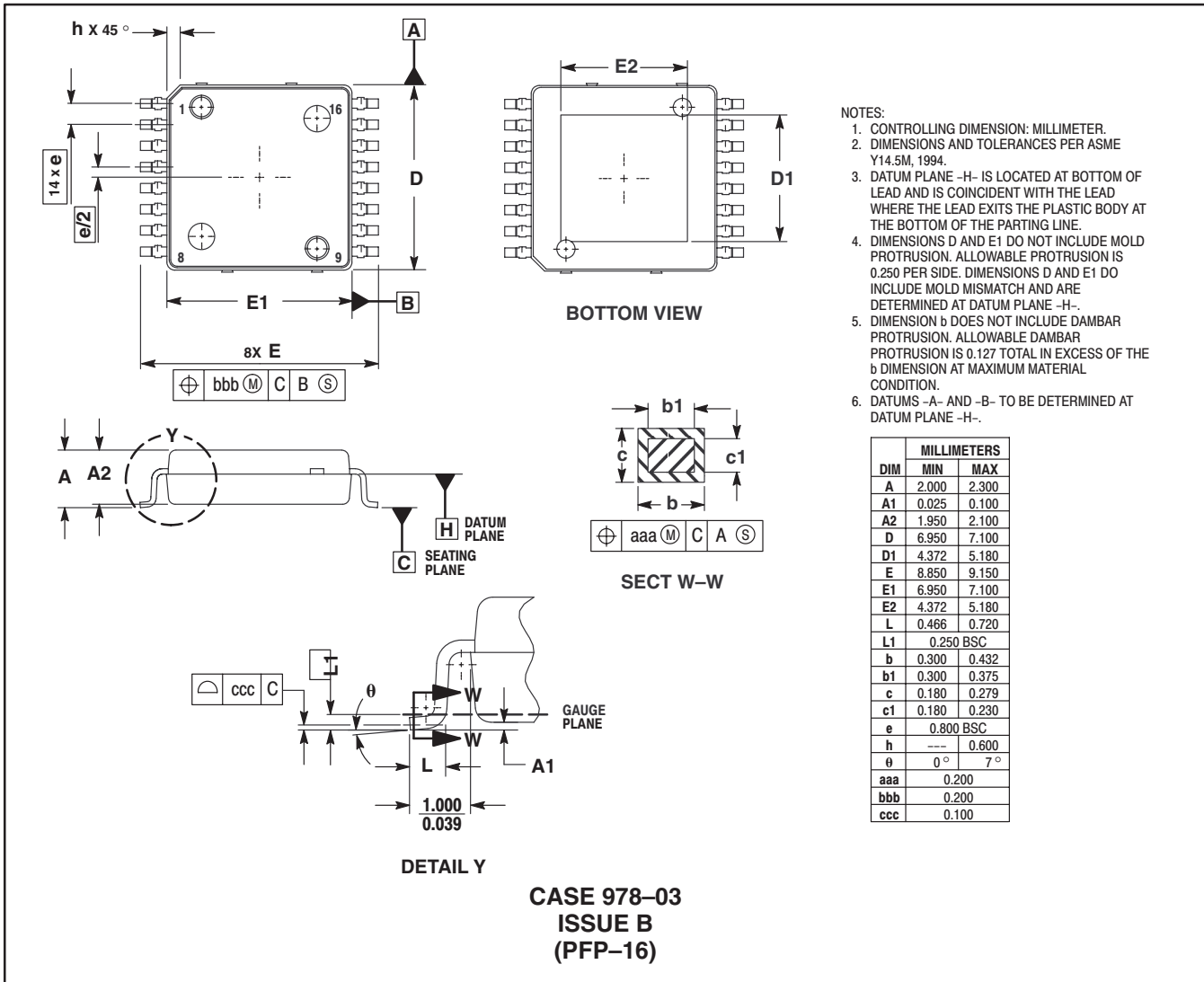


Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, and drain efficiency.

Figure 22. Large Signal Impedance

PACKAGE DIMENSIONS



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