8K x 8 RADIATION-HARDENED STATIC RAM - SOI HX6364

FEATURES

RADIATION

- Fabricated with RICMOS™ Silicon on Insulator (SOI) 1.2 μm Process
- Total Dose Hardness through $1x10^5$ rad(SiO_2)
- Neutron Hardness through $1x10^{14}$ cm^{-2}
- Dynamic and Static Transient Upset Hardness through $1x10^{11}$ rad(Si)/sec
- Soft Error Rate $<1x10^{-10}$ upsets/bit-day
- Dose Rate Survivability through $1x10^{13}$ rad(Si)/sec
- Latchup Free

OTHER

- Full military temperature operation (-55°C to 125°C)
- Access Time ≤ 45 ns (-55°C to 125°C)
- Low Power Disabled Mode
- Low Operating and Standby Current
- Data Retention down to 2.5 V
- Asynchronous Operation
- TTL/CMOS Compatible I/O
- High Output Drive
- Tri-State Outputs
- Single 5 V ± 10% Power Supply

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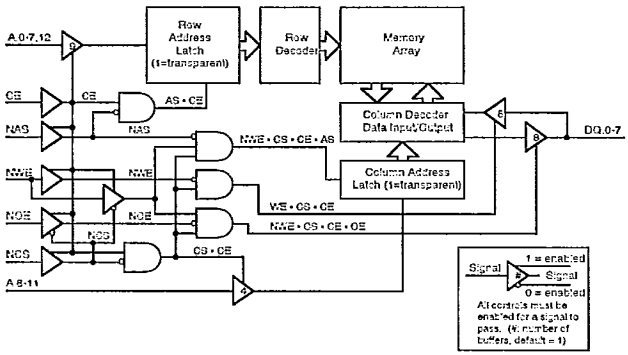
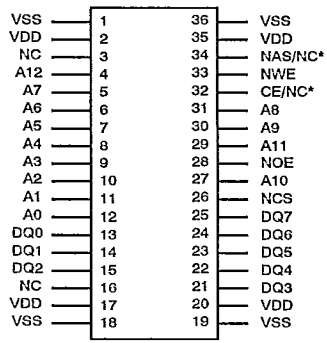
FUNCTIONAL DIAGRAM



PINOUT CONFIGURATION



NC = no connect
* Package pin configuration option

TRUTH TABLE

NCS	CE	NWE	NOE	NAS	MODE	DQ
L	H	H	L	X	Read	Data Out
L	H	L	X	X	Write	Data In
H	X	X	XX	X	Deselected	High Z
XX	L	XX	XX	XX	Disabled	High Z

Notes: X : VI=VIH or VIL
XX : VSS≤Vi≤VDD
NAS=L: Address latches are transparent
NAS=H: Address latches are closed
NOE=H: High Z output state maintained for NCS=X, CE=X, NWE=X, or NAS=X.

PACKAGE DESIGN

The 8Kx8 is offered in a custom 36-lead flat pack or a standard JEDEC 28-lead DIP (pinout not shown). Both package bodies are constructed of multilayer ceramic (Al_2O_3) and contain internal power and ground planes to minimize the effect of transient radiation environments. The package lids are made of Kovar.

DC and AC ELECTRICAL CHARACTERISTICS (1,2)

Symbol	Parameter	Min	Max	Units	Test Condition
IDDSB	Static Supply Current		450	µA	VIH/VIL=VDD/VSS IO=0, Inputs Stable
IDDOP	Dynamic Supply Current		8	mA/MHz	All inputs switching
IDDSEI	Static Supply Current - per TTL/CMOS Input		30	µA/Input	VIH = VDD-0.5 V VIL = 0.5 V
VIL	Low-Level Input Voltage - TTL		0.8	V	
VIH	High-Level Input Voltage - TTL	2.2		V	
VIL	Low-Level Input Voltage - CMOS		$0.3*V_{DD}$	V	
VIH	High-Level Input Voltage - CMOS	$0.7*V_{DD}$		V	
VOL	Low-Level Output Voltage		0.4 0.1	V	IOL = 10 mA IOL = 20 µA, VDD=4.5V
VOH	High-Level Output Voltage	4.2 VDD-0.1		V	IOH = -5 mA IOH = -20 µA, VDD=5.5V
II	Input Leakage Current	-5	5	µA	VSS≤VI≤VDD
IOZ	Output Leakage Current	-10	10	µA	VSS≤VIO≤VDD Output=high Z
TAVQV	Address Access Time - Read (-55 to 125°C)		45	ns	(3)
TAVQV	Address Access Time - Read (0 to 80°C)		40	ns	(3)
TAVWH	Address Valid to End of Write Time (-55 - 125°C)		45	ns	(3)
TAVWH	Address Valid to End of Write Time (0 - 80°C)		40	ns	(3)

(1) For timing diagrams and Absolute Maximum Ratings see the HC6364 data sheet.
(2) Worst case operating conditions: VDD=4.5 V to 5.5 V, TA=-55°C to +125°C, total dose through $1x10^6$ rad(SiO_2) unless noted otherwise
(3) Input levels VIL/VIH=0.0/3.0V(TTL) and VIL/VIH=0.5/VDD-0.5V(CMOS), input rise and fall times <5ns, input and output timing reference =1.5V(TTL) and VDD/2(CMOS), output loading=50pF

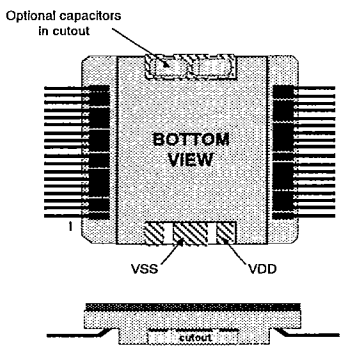
ORDERING INFORMATION

H X 6364/1 X S H Z C

- **SOURCE** H=HONEYWELL
- **PROCESS** X=SIMOX
- **PART NUMBER (3)**
- **PACKAGE DESIGNATION** X=36-Lead Flat Pack, R=28-Lead DIP, - = Bare Die (No Package)
- **SCREEN LEVEL** C=Brass Board, S=Modified Class S (1)
- **RADIATION HARDNESS** H=1E6 rad(SiO_2)
- **SOFT ERROR RATE (2)** Z=<1E-10 upsets/bit-day
- **INPUT BUFFER TYPE** C=CMOS Levels, T=TTL Levels

(1) Refer to the HC6364 data sheet for Honeywell screening procedures.
(2) SER spec. indicate worst case, high temperature (125°C), post-total dose performance.
(3) Contact factory for optional pinouts available.

This data sheet contains specifications based on development level information and may be subject to change upon completion of full characterization. Honeywell reserves the right to make changes to any products herein to improve reliability, function or design. Honeywell does not assume liability arising out of the application or use of any product or circuit described herein neither does it convey any license under its patent rights nor the rights of others.



36 - LEAD FLAT PACK

Optional stiffening capacitors can be mounted on the backside of the package in the cutout area. This helps to reduce supply rail collapse under transient upset conditions.

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