PRODUCT BRIEF

AHA G709D-10 FEC Core

10 GB/S ITU G.709 REED-SOLOMON DECODER

After more than 15 years building leading edge Reed-Solomon ICs, AHA is licensing its patented technology for the first time. The G709D-10 core implements the 16 block interleaved RS(255,239) code specified by in Annex A of the ITU G.709 standard.

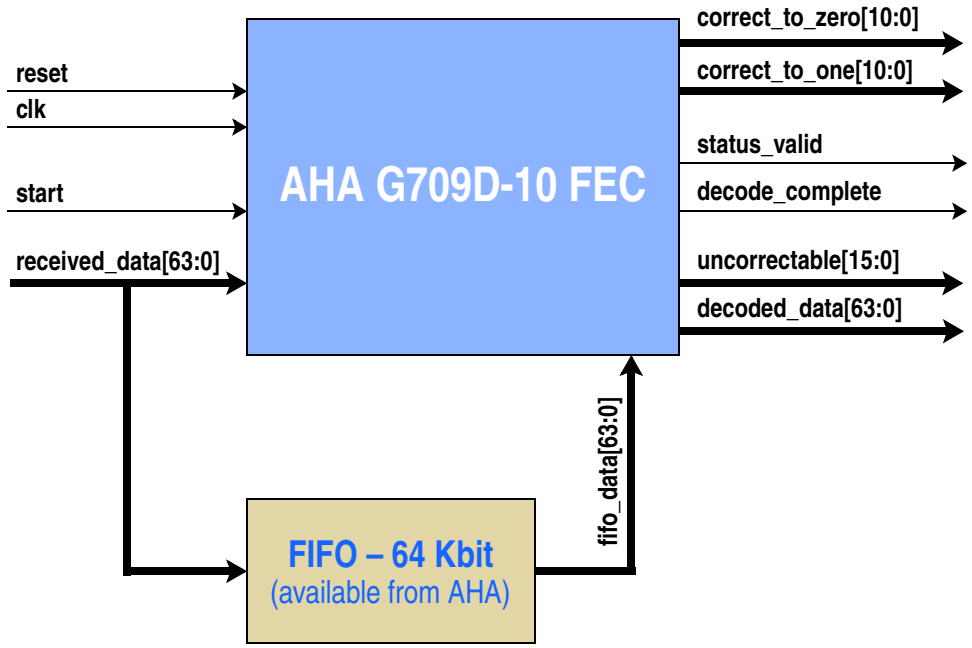
The G709D-10 core is specifically designed to efficiently perform the Reed-Solomon decoding function specified by the standard. The core requires no configuration, no initialization, and no re-synchronization procedure or includes any unnecessary features that would add area, power or complexity to your design.

A complementary G709E RS encoder is also available from AHA.

FEATURES

- ITU G.709 Compatible Reed-Solomon core
- Input and output data streams are block-interleaved for seamless connection in G.709 system
- 10 Gbits/sec operation in 0.18µ CMOS process
- 140 Kgates in 0.18µ using a typical standard cell library
- Less than 100 mA of dynamic current in UMC's 0.18µ CMOS process
- One-edge, one-clock fully synchronous design without multi-cycle paths
- Separate FIFO for increased flexibility and simplified IC floor planning
- Complete error reporting for Bit Error Rate calculation and feedback into threshold detection circuits

Figure 1: AHA G709D-10 FEC



comtech aha corporation

INPUT SIGNALS

clk - 166 MHz core clock. All inputs are registered on the rising edge.

reset - Synchronous reset.

received_data[63:0] - Received data bus. Data bus is valid every clock and is registered on the rising edge of **clk**. The data frame is restarted whenever **start** is active. The core accepts 8-bytes per transfers

start - Signal is active to when the first 8 bytes of the G.709 frame in on the **received_data** bus. Must be inactive on all other data transfers in the frame. Maybe asserted at anytime of the data frame needs to be reset to the first transfer.

fifo_data[63:0] - FIFO data. Delay version of the **received_data** data stream. The bus is registered on the rising edge of **clk**.

OUTPUT SIGNALS

decode_complete - Decoding complete. Active when the first 8-byte transfer of the G.709 frame is on the **decode_data** data bus and inactive on all subsequent transfers.

decoded_data[63:0] - Decoded data. The first 8-bytes of the corrected G.709 frame are valid when **decode_complete** is active and the remainder of the frame is available over the subsequent 509 clocks. The data is driven from the rising edge of **clk**.

status_valid - Status valid signal. Active for a single **clk** following the completion of the frame to indicate when the **uncorrectable**, **correct-to-zero**, and **correct_to_one** signals are valid.

uncorrectable[15:0] - Uncorrectable block flags. Each bit of the signal corresponds to one of the 16 Reed-Solomon blocks in the G.709 frame. Valid when **status_valid** is active.

correct_to_zero[10:0] - Number of bits corrected from '1' to '0' in the just completed G.709 frame. Signal is valid when **status_valid** is active.

correct_to_one[10:0] - Number of bits corrected from '0' to '1' in the just completed G.709 frame. Signal is valid when **status_valid** is active.

DELIVERABLES

- G.709D-10 FEC core (VHDL)
- Timing constraints (DesignCompiler and Ambit format)
- Test bench and verification vectors (VHDL)
- Single use license to AHA's Reed-Solomon Patents

PATENTS

Design uses one or more of the following US Patents: 5,170,399; 5,099,482; 4,873,688; 5,396,502

CONTACT INFORMATION

Comtech AHA Corporation
2345 NE Hopkins Court
Pullman WA 99163
(509) 336-7115
sales@aha.com
http://www.aha.com

comtech aha corporation
A subsidiary of Comtech Telecommunications Corporation
2345 NE Hopkins Court ▪ Pullman, WA 99163-5601
tel: 509.334.1000 ▪ fax: 509.334.9000
e-mail: sales@aha.com ▪ www.aha.com