

Radiation Hardened High Speed Dual Voltage Comparator

The ISL7119RH is a radiation hardened high speed dual voltage comparator fabricated on a single monolithic chip. It is designed to operate over a wide dual supply voltage range as well as a single 5V logic supply and ground. The open collector output stage facilitates interfacing with a variety of logic devices and has the ability to drive relays and lamps at output currents up to 25mA.

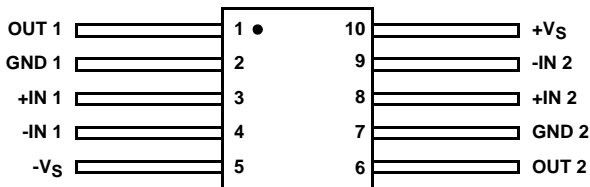
The ISL7119RH is fabricated on our dielectrically isolated Rad-hard Silicon Gate (RSG) process, which provides immunity to Single Event Latch-up (SEL) and highly reliable performance in the natural space environment.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the ISL7119RH are contained in SMD 5962-07215. A “hot-link” is provided on our website for downloading.

Pinouts

ISL7119RH
(10 LD FLATPACK GDFP1-F10 OR CDFP2-F10)
TOP VIEW



Features

- Electrically Screened to DSCC SMD # 5962-07215
- QML Qualified Per MIL-PRF-38535 Requirements
- Radiation Environment
 - Total Dose. 3 x 10⁵ RAD(Si)
 - SEL/SEB. Immune
- Input Offset Voltage (V_{IO}). 8mV (Max)
- Input Bias Current (I_{BIAS}) 1000nA (Max)
- Input Offset Current (I_{IO}) 150nA (Max)
- Saturation Voltage @ I_{SINK} = 3.2mA (V_{SAT}) . 0.65V (Max)
- Saturation Voltage @ I_{SINK} = 25mA (V_{SAT}) . . 1.8V (Max)
- Response Time (t_{PD}) 160ns (Max)

Applications

- Window Detector
- Level Shifter
- Relay Driver
- Lamp Driver

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
5962F0721501QXC	ISL7119RHQF	Q 5962F07 21501QXC	-55 to +125	10 Ld Flatpack	K10.A
5962F0721501VXC	ISL7119RHVF	Q 5962F07 21501VXC	-55 to +125	10 Ld Flatpack	K10.A
5962F0721501V9A	ISL7119RHVX		-55 to +125	10 Ld Flatpack	K10.A
ISL7119RH/Proto	ISL7119RHF/Proto	ISL7 119RHF /Proto	-55 to +125	10 Ld Flatpack	K10.A

Die Characteristics

DIE DIMENSIONS:

2030µm x 2030µm (~80 mils x 80 mils)
 Thickness: 483µm ± 25.4µm (19 mils ± 1 mil)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorous Silicon Glass)
 Thickness: 8.0kÅ ± 1.0kÅ

Top Metallization:

Type: AlSiCu
 Thickness: 16.0kÅ ± 2kÅ

Substrate:

Radiation Hardened Silicon Gate, Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION:

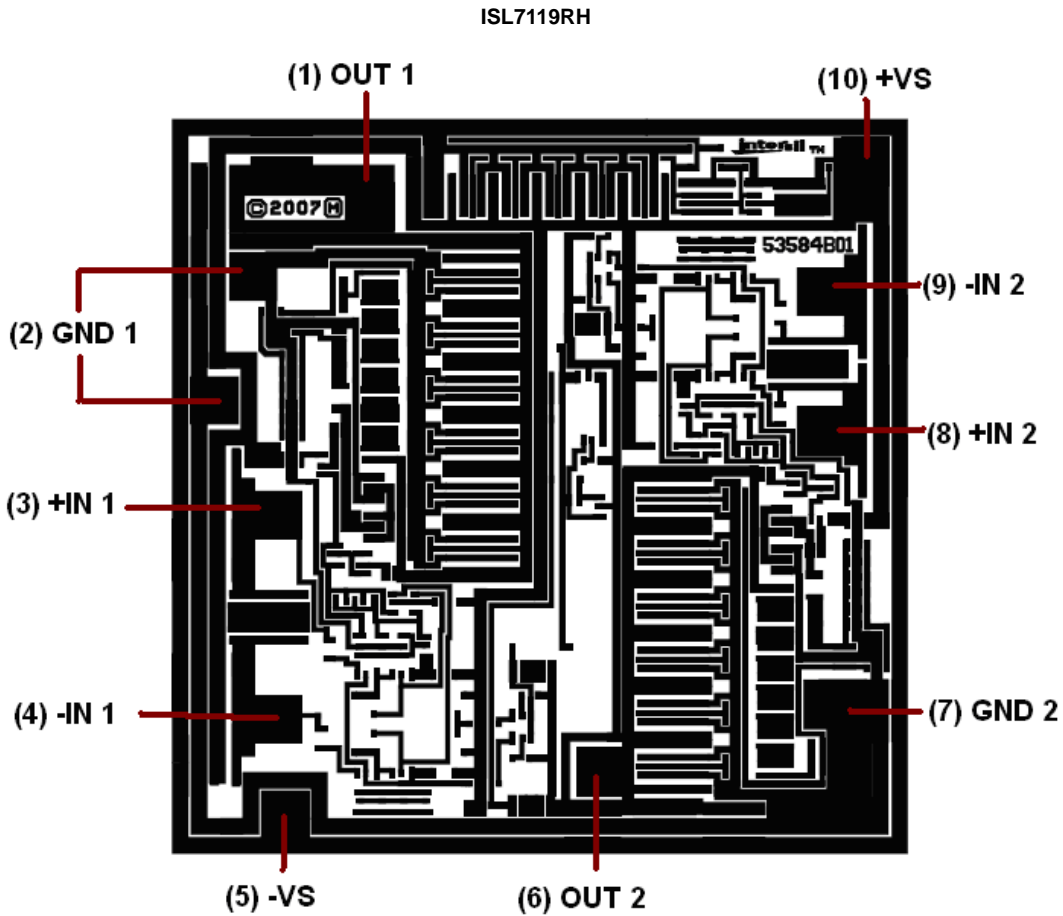
Worst Case Current Density:

<2.0 x 10⁵ A/cm²

Transistor Count:

66

Metallization Mask Layout



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com